DISSIPATION FACTOR OF CERAMIC CAPACITORS; A PRIMER

What is DF and how does it impact my application?

Simply stated, DF is a measure of power lost traveling through a capacitor. This loss is mainly in the form of heat, which compounds the loss as the resulting temperature rise can cause additional problems such as:

- Diminished life of the capacitor and other circuit elements near it.
- Deterioration of electrical properties of other components affected by the temperature increase, such as change in resistivity, reactance, voltage or current carrying capability, etc.
- Smoking
- In extreme cases total component destruction can occur resulting in fire or explosion.
- Increase in circuit weight due to necessity to reduce the temperature rise by use of heat sinking or fans. Of course, this is particularly problematic in aircraft and aerospace applications.

What is the cause of DF?

Again, simply stated, DF is caused by two items; Dielectric Loss, a property of the particular ceramic formulation used and (Series) **Resistance, Resistance, Resistance**, both internal and external to a capacitor. Some of the places this resistance can occur are:

Internal

- Electrodes; commonly used materials are precious metals such as silver, palladium, palladium silver and various other alloys. Also used (for cost reduction) are base metals such as copper and nickel. Each of these materials has its own resistivity which is directly proportional to resistance.
- Terminations; same considerations as electrodes except that they also contain a glass frit to bring about bonding between the termination and the ceramic element.

External

- Plating and/or solder applied to the terminations of capacitor chips to enhance solderability.
- Leads
- Circuit board pads and conductors
- Material used to attach chips to board (solder, conductive adhesive, etc.)

Internal and External

Joint resistance where any two of the aforementioned constituents meet. e.g.

- Electrode – Termination
- Termination – Plating

- Plating – Solder
- Solder – Circuit board
- Termination – Conductive epoxy – circuit board
- Termination – Lead – Circuit

What is DF mathematically? How can I minimize its impact in my application?

In a capacitor, DF is the ratio of series resistance to capacitive reactance. From the following analysis it can be seen that that for a given circuit, Series Resistance, Rs, is the driving factor for DF and DF is directly proportional Rs.

$DF = Rs/Xc$

$Xc = 1/2 \pi F C$

Hence, $DF = 2 \pi F C Rs$

Where F = Frequency in Hertz

C = Capacitance in Farads

Rs = Series Resistance in Ohms

Xc = Capacitive reactance

The first step towards minimizing the affects of DF in your circuit is to choose the highest Q dielectric you have the room for. As nature would have it, the best ones are usually produce the largest caps, but bear in mind the overall impact on size and weight. For example, you could pick a smaller cap with a higher DF but have to heat sink it. This could more than negate the weight advantage gained by use of a smaller sized unit. Once you've selected the cap, use the lowest resistance materials to attach it to your circuit which itself should have the lowest resistivity conductors.

How does Q enter into this?

Q is the mathematical reciprocal of DF and thus increases as DF decreases. It is used for that reason; the best part will have the highest Q. This is illustrated by the following table:

Capacitor type	Cap, pf	F, Mhz	Rs, milliohms	DF	Q
Paper/foil	100	1	1	0.062830	15.9
Ceramic X7R	100	1	0.4	0.025132	39.8
Typical NP0	100	1	0.015	0.000942	1061.1
MCI Hi Q	**100**	**1**	**0.0015**	**0.000094**	**10610.6**
Ceramic X7R	1000	10	0.004	0.025132	39.8
Typical NP0	1000	10	0.00015	0.000942	1061.1
MCI Hi Q	**1000**	**10**	**0.000015**	**0.000094**	**10610.6**

Conclusions

Series Resistance (any resistance in series with your capacitor) is the power robbing, Q killing culprit. There are many steps you can take to minimize it, starting with your original module design.

- Allow enough room to accommodate the highest Q capacitor you can.
- Design your boards to have the highest conductivity pads and conductors even if it means using more expensive materials and/or thicker patterns. Use the shortest and widest conductors you can.
- Chose the chip attachment method and material with the least resistance. Make sure that the joint is solid and void free. Voids in joints are big contributors to Rs.
- If wire leads are to be used they should be made of very low resistivity material and have minimum length and maximum diameter. Attachment should be made with a high conductivity alloy and ample fillet.